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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,108	04/14/2000	Thomas M. Olson	SRT-001	8462

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EXAMINER
BATAILLE, PIERRE MICHE

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,108	OLSON, THOMAS M.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-23* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4, 5, 6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-19 are presented in the application for examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on February 26, 2001; February 4, 2002, and April 22, 2002 was in the application (Paper No. 4, 5, and 6, respectively. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The following objection is noted:

"a" should b replace with – the --, claim 1, line 8.

" a " in both occurrences in claim 2 should be replace with "the" for consistency.

"the start" should be replaced with -- a start --, claim 16.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 11, 13-14, 19-21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,694,583 (Williams et al).

With respect to claim 1, William teaches a computer system with an operating system (DOS (disk operating system) executed by a CPU) and persistent memory (system memory) [Col. 4, Lines 32-44], comprising: a memory comprising: a non-persistent memory region (region other than protected region of the memory system), directly accessible by the operating system (provided conventional memory accesses (read/write/clear operations)); and a persistent memory region (protected region of the memory system; space in storage area for preserving BIOS emulation parameters) [Col. 4, Lines 25-29]; and an intermediary program (command for worm boot) in communication with the operating system and the persistent memory region, wherein the intermediary program enables the operating system to address a persistent memory region [Col. 4, Lines 48-58; Lines 25-39].

With respect to claims 2, Williams teaches the non-persistent memory (Floppy, hard disk, CD-ROM, non-volatile memory) and the persistent memory (main or system memory) are different physical memory [Col. 5, Line 54 to Col. 6, Line 20].

With respect to claim 3, Williams teaches the intermediary program being a device driver (BIOS included within the CPU for carrying prescribed functions including converting operating signals developed by the operating system executed by the CPU into signals compatible with devices) [Col. 8, Lines 46-50].

With respect to claim 4, William teaches a basic input/output system (BIOS), which prevents direct access to the persistent memory region by the operating system (BIOS included within the CPU for carrying prescribed functions including converting operating signals developed by the operating system executed by the CPU into signals compatible with devices) [Col. 8, Lines 46-50].

With respect to claim 5, Williams teaches the persistent memory region allocated to redundant CPU memory locations [parameters moved from BIOS to protected memory region; protected volatile memory region of said system memory and responsive to a command for a warm boot for duplicating and preserving the media emulation parameters; Col. 4, Lines 56-59; Col. 7, Lines 8-12].

With respect to claims 11, 13, 20-21 and 23, the claims recite features similar to claim 1. Therefore, Williams' disclosure meets the features of these claims.

With respect to claim 14, Williams teaches the contents of the persistent memory region retain their integrity during a boot cycle [Col. 4, Lines 56-59; Col. 7, Lines 8-12].

With respect to claim 18-19, William teaches the recited first, second and third memory regions, as described in claim 18 [Fig. 1, 5-7, and 12], and the operating system being DOS which is a Microsoft operating system.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-9 rejected under 35 U.S.C. 103(a) as being unpatentable over 5,694,583 (Williams et al) in view of US 5,383,161 (Sanemitsu).

With respect to claims 6-9, William teaches the invention as claimed, but fails to teach a non-volatile memory or a file containing information concerning configuration of the persistent and/or the non-persistent memory. However, Sanemitsu teaches an IC card including a semiconductor memory having a non-writable memory region which does not permit overwriting and a writable memory region which permits overwriting of stored data [Abstract], wherein the IC card further includes a second semiconductor memory storing physical information concerning the IC card, such as capacity of the memory and access time [abstract; Col. 2, Lines 57-63]. Therefore, it would have been obvious to one having ordinary skill in the art and having both teachings before him at the time of the invention, to include, into the system of William, the non-volatile memory or file containing information concerning configuration of the persistent and/or the non-persistent memory, as taught by Sanemitsu because the result would have permitted proper access control of the memory card, as taught by Sanemitsu [Col. 2, Lines 26-34].

8. Claims 10, 15, and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over 5,694,583 (Williams et al) in view of McNutt et al (US 5,799,324).

With respect to claims 10, 15, and 22, Williams teaches the invention as claimed, but fails to specifically teach a look-aside buffer for buffering write requests. However, McNutt teaches a storage device partitioned into a persistent storage area and non-persistent storage area, using a collection buffer for staging write requests [Abstract; Col. 2, Line 66 to Col. 3, Line 3; Col. 3,Lines 49-53]. Therefore, it would have been obvious to one having ordinary skill in the art and having both teachings before him at the time of the invention, to include, into the system of William, look-aside buffer for buffering write requests, as taught by McNutt because the result would have permitted continually fast accesses over a long period of time, as taught by McNutt.

9. Claims 16-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,694,583 (Williams et al) in view of US 5,875,465 (Kilpatrick et al).

With respect to claims 16-17, Williams teaches the invention as claimed, but fails to specifically teach defining start address of each, the persistent storage area and non-persistent storage area. However, Kilpatrick teaches a memory cache array having a programmably sized portion locked down so that it is not replaced and the complementary programmable range portion where overwriting takes place [abstract; Col. 3, Lines 1-6]. Therefore, it would have been obvious to one having ordinary skill in the art and having both teachings before him at the time of the invention, to include into the system of William, the defining start address of each, the persistent storage area

and non-persistent storage area, as taught by Kilpatrick because the result would have permitted dynamic partition of the storage area to be locked down and the dynamic partition of the storage area where overwriting takes place [Col. 3, Lines 12-17].

Allowable Subject Matter

10. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

EP 0 461 924 A2 (Kelley et al) teaching circuitry for determining cacheable address and write-protect memory address regions in a computer system includes a programmable limit register associated with each respective memory address region, defining a boundary limit for each of the respective memory regions.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone

numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Pierre-Michel Bataille
Examiner
Art Unit 2186

June 14, 2003